UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/443,160 | 11/19/1999 | DAVID L. ISAMAN | 98-MET-069 | 6854 |

30425 7590 07/10/2009

STMICROELECTRONICS, INC.
MAIL STATION 2346
1310 ELECTRONICS DRIVE
CARROLLTON, TX 75006

| EXAMINER | |
|---|---|
| ALROBAYE, IDRISS N | |
| **ART UNIT** | **PAPER NUMBER** |
| 2183 | |

| MAIL DATE | DELIVERY MODE |
|---|---|
| 07/10/2009 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/443,160 | ISAMAN, DAVID L. | |
| | Examiner | Art Unit | |
| | IDRISS N. ALROBAYE | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *21 April 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *2,3,6-13 and 16-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-3, 6-13, 16-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Amendment*

1. This action is responsive to amendments filed 4/21/2009.

2. Claims 2-3, 6-13, 16-21 remained for examination. Claims 1, 4-5 and 14-15 are canceled.

3. Applicant's amendments to claims 2-3 and 12-13 to overcome 35 USC 112 2nd paragraph rejections have been considered and the rejections have been withdrawn.

### *Claim Objections*

4. Claim 20 is objected to because of the following informalities: the "*first memory location **nd** the second...",* should be changed to "*first memory location **and** the second…*". Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

5. The following is a quotation of the first and second paragraphs of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
>
> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 2-3, 6-13 and 16-19 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably

convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

7. As per claims 2 and 12, taking claim 2 as exemplary, the claim recites "*without computing a memory address equaling the first base address value added to the offset address values in detecting the first instruction*", this limitation is a new matter which was not described in the specification in such a way as to reasonably convey to one skilled in the art that the inventors, at the time the application was filed, has possession of the claimed invention. There is no basis in the original disclosure for detecting the first instruction without computing a memory address equaling the first base address added to the offset address values. (see also response to arguments for more details)

Note that obviousness is not the test for written description. As stated in Lockwood v. American Airlines, Inc., 107 F.3d 1565, 1572, 41 USPQ2d 1961, 1968 (Fed. Cir. 1997):

> The question is not whether a claimed invention is an obvious variant of that which is disclosed in the specification. Rather, a prior application itself must describe an invention, and do so in sufficient detail that one skilled in the art can clearly conclude that the inventor invented the claimed invention as of the filing date sought. See Martin v. Mayer, 823 F.2d 500, 504, 3 USPQ2d 1333, 1337 (Fed. Cir. 1987) (stating that it is "**not a question of whether one skilled in the art might be able to construct the patentee's device from the teachings of the disclosure.... Rather, it is a question whether the disclosure necessarily discloses that particular device**.") (quoting Jepson v. Coleman, 50 C.C.P.A. 1051, 314 F.2d 533, 536, 136 USPQ 647, 649-50 (1963))..... One shows that one is "in possession" of the invention by describing the invention, with all of its claimed limitations, not that which makes it obvious.

8. As per claims 3 and 13, the claims recite a second instruction instead of the first instruction but includes similar features as in claim 2. Therefore claims 3 and 13 are rejected for the same reasoning as set forth above in claim 2.

### *Claim Rejections - 35 USC § 102*

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 2, 12 and 20 are rejected under 35 U.S.C. 102 (b) as being anticipated by Yeager U.S. Patent No. 6,216,200.

11. As per claim 20, Yeager teaches a method for operating a pipelined microprocessor, comprising:

detecting a first instruction that stores data to a first memory location (see col. 8, lines 1-14, “store instruction”), the first instruction comprising syntax for computing an effective address for the first memory location (see col. 5, lines 13-26, wherein “virtual address” is equivalent to syntax; see also col. 9, lines 18-39, "offset" is equivalent to effective address);

detecting a second instruction that loads data from a second memory location (see col. 28, lines 54-65, “load instruction”), the second instruction comprising syntax for computing an effective address for said second memory location (see col. 5, lines 13-

26, wherein “virtual address” is equivalent to syntax; see also col. 9, lines 18-39, "offset" is equivalent to effective address);

determining the syntax for said the first instruction and the syntax for said the second instruction (see col. 30, lines 43-49 comparison of "virtual addresses");

using the syntax for said the first instruction and said the syntax for the second instruction to determine a relationship between the first memory location and the second memory location (see col. 30, lines 43-49 comparison of "virtual addresses" to see if there’s store-to-load dependency), without using the effective address of the first memory location or the effective address for the second memory location (see col. 30, lines 43-49. First virtual address are not effective addresses, thus it's "without using the effective addresses". Second, this limitation is interpreted as without using effective address to access memory which is shown in col. 30, lines 43-65) to determine the relationship between the first memory location and the second memory location (see col. 30, lines 43-49 checking if there’s store-to-load dependency); and

using the relationship to determine whether to perform one of the first instruction and the second instruction (col. 30, lines 43-65).

12. As per claim 2, Yeager teaches a pipelined microprocessor detecting a first instruction using first base and offset address values to load data from a first memory location that was previously stored to (see col. 28, lines 54-65 “load and store”; see col. 5, lines 13-26 and col. 9, lines 18-39, "offset" and “base”), wherein the first instruction is detected based upon the first base and offset address values (see col. 30, lines 43-49

"comparison of virtual addresses") and without computing a memory address equaling the first base address value added to the offset address values in detecting the first instruction (see col. 30, lines 43-49 comparison of "virtual addresses" to see if there's store-to-load dependency. There is no memory address computation equaling the first base address value added to the offset address values, thus reads on the limitation; see also abstract wherein the dependencies is detected before virtual address calculation).

13. As per claim 12, it is rejected for the same reasons set forth above in claim 2.

14. Claims 2-3, 6-13, 16-21 are rejected under 35 U.S.C. 102 (b) as being anticipated by Hesson et al. U.S. Patent No. 5,666,506 (hereinafter Hesson).

15. As to claim 2, 12, Hesson taught at least:

A pipelined microprocessor (see pipeline processor in col. 1, lines 29-34 for background) detecting a first instruction using first base and offset address values to load data from a first memory location that was previously stored to (see comparison of instruction in col. 4, lines 64-67 and col. 5, lines 1-13, wherein the virtual address has a base and effective address), wherein the first instruction is detected based upon the first base and offset address value and without computing a memory address equaling the first base address value added to the offset address values in detecting the first instruction (see col. 4, lines 65-67, that there is not computation of memory address

equaling the first base address value added to the offset address values in detecting the first instruction).

16. As to Claims 3, 13, Hesson taught detecting a second instruction that stores data into a second memory location that was previously read from without computing a memory address equaling the first base address value added to the offset address values in detecting the first instruction (see store address being compared to all load addresses in col.6, lines 13-15 and 35-41).

17. As to claims 6, 7, 16, 17, Hesson's virtual addresses were examined to access memory location (see virtual address in col.4, lines 64-67).

18. As to claim 8, 9, 18, 19, examiner holds that virtual same address must have identical base and identical offset.

19. As to claim 10, 11, Hesson also taught a bypass element [violation condition] capable of sending a bypass signal to an instruction execution stage of pipelined microprocessor that indicates that instructions referred to an identical memory location (see store violation condition detected in col.6, lines 35-42).

20. As to claims 20, Hesson also taught at least

a) detecting a first instruction that stores data to a first memory location, said first instruction comprising syntax (see virtual address comparison) for computing an effective address for the first memory location and the operands needed to compute the effective address in (see the store instruction for the first instruction in store barrier hit detection in col. 5, lines 3-13, see the virtual addresses as the syntax);
b) detecting a second instruction that loads data from a second memory location, the second instruction comprising syntax for computing an effective address for said second memory location (see the snoop of the load instruction as the second instruction in col.6, lines 13-21).

21. Hesson did not explicitly show the determination of syntax relationship between the first memory location and said second memory location, without using the effective address per se as argued by applicant. However, Hesson teaches without using the effective address of the first memory location or the effective address of the second memory to determine the relationship between the first memory location and the second memory location (see co1.4, lines 56-67, co1.5, lines 1-13). As explained in the response to arguments, "*using the effective address of the first memory location*" is interpreted as using the effective address to access memory location.

22. As to the detection of the instructions, examiner holds that for the purpose of detecting the load/store conflicts, Hesson must detect the op code of an instruction to

see whether it was a load or store instruction, and virtual addresses by the instructions must comprise a syntax for computing effective address of memory location.

23. As to claim 21, Hesson was also directed to identical memory location (see the address conflicts in col.6, lines 3-29).

### *Response to Arguments*

24. Applicant's arguments filed 4/21/2009 have been fully considered but they are not persuasive.

25. **Appellant's Argument**:

"Applicant argues 35 USC 112 1st rejection with respect to previous claim language of claims 2-3 and 12-13, however the claims have been amended to recite "*without computing a memory address equating the first base address value added to the offset address values in detecting the first instruction".* The applicant refers back to the specification to support this claim amendment. Specifically applicant refers to "*When the bypass signal is generating, the address computation stage 130, does not have to compute the actual effective address for the microprocessor 100 to act on the knowledge that the instructions 151 refer to identical locations in external memory".*

**Examiner's Response**:

The examiner respectfully disagrees. The claim language indicates that in detecting the first instruction, it does not compute a memory address to equaling the first base address added to the offset address values. However, the specification shows that **after** the first instruction has been detected it does not generate the actual effective address. Furthermore, the specification does not show computing memory address

equaling the first base address added to the offset address values with respect to the negative limitation "*without computing...".*

Also as indicated above, obviousness is not the test for written description and it is not a question of whether one skilled in the art might be able to construct the patentee's device from the teachings of the disclosure…Rather, it is a question of whether the disclosure necessarily discloses that particular device.

26. **Applicant's Arguments**:

"Independent claims 2 and 12 each recite detecting a first instruction using first base and offset address values to load data from a first memory location that was previously stored to, wherein the first instruction is detected based upon the first base and offset address values and without using a memory address equaling to the first base address value added to the offset address value. Such a feature is not found in the cited references. *Yeager* teaches comparing virtual addresses that are, for indexed address calculations, formed by "base+index." *Yeager* column 9, lines 21-22. *Hesson et al* does not, as asserted in the Office Action, teach that the virtual addresses employed have base and effective addresses"

**Examiner's Response**:

With regards to Yeager references, the examiner respectfully disagrees because Yeager (abstract) clearly indicates that "*dependencies are tracked before virtual addresses are* ***actually calculated".*** Therefore, the dependencies of memory access instructions are detected before computing a memory address and thus reads on claimed language "*without computing a memory address..."*

With regards to Hesson, the bits of the virtual address that are used for comparison are considered to be equivalent to the base and offset address. However,

the virtual address of Hesson is not computed by adding two addresses (base plus offset).

27. **Applicant's Arguments**:

"Claim 20 recites using the syntax for the first instruction and the syntax for the second instruction to determine a relationship between the first memory location and the second memory location, without using the effective address for the first memory location or the effective address for the second memory location. Such a feature is not found in the cited references. Both *Yeager* and *Hesson et al* teach using the virtual addresses - that is, the effective addresses, as opposed to the physical or "real" addresses - of memory locations to determine correspondence of two memory locations. The interpretation of "using the effective address for the first memory location" as being limited to "using the effective address to access the memory location is arbitrary and capricious. No basis for such as limitation, other than to contrive a basis for rejection of the claim, exists."

**Examiner's response**:

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., physical or real addresses) are not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Furthermore, virtual addresses are equivalent to the claimed memory addresses. Also, as indicated by both references, virtual addresses are mapped to physical address (see for instance, Yeager, col. 5, lines 20-23).

***Conclusion***

28. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

29. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Amerson et al. (5,475,823) is cited for the teaching of detection circuit [520] detecting the load instruction accessing a location previously stored (see fig.5, 4, lines 55-67, co1.8, lines 10-24, lines 37-48);

b) Kiyohara et al. (5,694,577) is cited for the teaching of comparison of virtual addresses of preload instructions and store instructions (see co1.2, lines 55-65, co1.5, lines 49-61 );

c) Ball (5,615,357) is cited for disclosure of a system including a determination of syntax relationship (see the model of CPU) without itself calculating effective addresses of the first a and second instructions (see the trace file containing the load and store instruction effective addresses in co1.2, lines 39-45, lines 64-67, col.3, lines 1-6, co1.4, lines 1-11, co1.11, lines 59-67, see co1.10, lines 10-52 for the trace driven mode, see co1.12, lines 1-7 for load and store).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to IDRISS N. ALROBAYE whose telephone number is (571)270-1023. The examiner can normally be reached on Mon-Fri from 8:00 to 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Idriss Alrobaye
AU 2183
(571) 270-1023

/Aimee J Li/
Primary Examiner, Art Unit 2183